Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims:

1. (Cancelled)
2. (Cancelled)
3. (Cancelled)
4. (Cancelled)
5. (Cancelled)
6. (Cancelled)
7. (Cancelled)
8. (Cancelled)
9. (Cancelled)
10. (Cancelled)
11. (Cancelled)
12. (Cancelled)
13. (Cancelled)
14. (Cancelled)
15. (Cancelled)
16. (Cancelled)
17. (Cancelled)
18. (Cancelled)

19. (Previously Presented) An equalization circuit, comprising:

an input adapted to receive signals from a communication channel;

an equalizer bank having at least two equalizers coupled in parallel and coupled to the input;

a first decoder bank having at least two packet decoder circuits coupled in parallel, each packet decoder circuit responsive to a corresponding one of the at least two equalizers of the equalizer bank;

a selector circuit coupled to the decoder bank that selects an output signal of one of the at least two equalizer circuits based on processing of the decoder bank;

an output coupled to the selector circuit that receives the selected output signal; and

a second decoder bank having at least two error correction decoder circuits coupled in parallel, each error correction decoder circuit coupled to a corresponding one of the at least two equalizers of the equalizer bank and coupled to a corresponding one of the at least two packet decoder circuits.

20. (Original) The equalization circuit of claim 19, wherein the second decoder bank includes at least two forward error correction decoder circuits.

21. (Cancelled)
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51. (Cancelled)

52. (Previously Presented) The equalization circuit of claim 19, wherein each of the at least two equalizers comprises one of a fixed equalizer and an adaptive equalizer.

53. (Previously Presented) The equalization circuit of claim 52, wherein each of the adaptive equalizers comprises one of a linear equalizer and a nonlinear equalizer.

54. (Previously Presented) The equalization circuit of claim 52, wherein each of the adaptive equalizers comprises one of a traversal structure and a lattice structure.

55. (Previously Presented) The equalization circuit of claim 19, wherein the first decoder bank provides a feedback signal to the at least two equalizers of the equalizer bank.

56. (Previously Presented) The equalization circuit of claim 55, wherein the feedback signal is also provided to the selector circuit to be used in selecting the output of one of the at least two equalizer circuits.

57. (Currently Amended) ~~The equalization circuit of claim 1, further comprising:~~ An equalization circuit, comprising:

an input adapted to receive signals from a communications channel;

a plurality of equalizer circuits coupled to the input and operable to generate a plurality of intermediate signals;

a selector circuit, responsive to the plurality of equalizer circuits, that selects one of the intermediate signals;

an output coupled to the selector circuit that receives the selected intermediate signal;

a plurality of buffer circuits, each buffer circuit coupled between one of the plurality of equalizer circuits and the selector circuit to buffer the intermediate signals for approximately the duration of a time slot of the communication channel; and

a plurality of error correction decoder circuits coupled in parallel, each decoder circuit coupled to a corresponding one of the plurality of equalizer circuits, wherein each of the plurality of buffer circuits is included in a corresponding one of the plurality of decoders.

58. (Previously Presented) The equalization circuit of claim 57, wherein each of the plurality of error correction decoder circuits is a forward error correction decoder circuit.

59. (Previously Presented) The equalization circuit of claim 57, wherein at least one of the plurality of error correction decoder circuits provides a feedback signal to at least one of the plurality of equalizer circuits.